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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/966,391	09/28/2001	Paul W. DeMone	MOSA-01001US1	6511

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EXAMINER	
NGUYEN, MINH T	
ART UNIT	**PAPER NUMBER**
2816	10

DATE MAILED: 02/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/966,391	DEMONE, PAUL W.	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 12-19* is/are rejected.

7)☒ Claim(s) *11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 March 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Applicant's response to the restriction requirement filed on 1/16/03 has been received and entered in the case. The following is a detailed Office Action.

Drawings

2. Figures 2A, 2B, 3A, 3B, 4A and 4B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

4. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

5. The abstract of the disclosure is objected to because it uses languages which can be implied, i.e., "Disclosed", "comprises". Correction is required. See MPEP § 608.01(b).

Claim Objections

6. Claim 9 is objected to because of the following informalities: line 14, "the power supply voltage" should be changed to -- a supply voltage received by the first and second pump cascades --. Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-8 and 12-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 1, the claim is rejected as being incomplete for failing to particularly point out the structural relationship between the recited plurality of charge pump cascades, i.e., the recitation is merely a "catalogue of elements". *See In re collier 158 USPQ 266.*

As per claims 2-3, these claims are rejected because of the indefiniteness of claim 1.

As per claim 4, the claim is rejected as being incomplete for failing to particularly point out the structural relationship between the recited first and second charge pump cascades, i.e., the first and second charge pump cascades are connected in parallel and one end of the connection is connected to an output node.

As per claims 5-8, these claims are rejected because of the indefiniteness of claim 4.

As per claim 12, the recitation of lines 12-13 appears misdescriptive because as shown in Fig. 5A of the present invention, stages 3 which are the final stages are not coupled in parallel, i.e., the inputs of the stages 3 are not seen as connected together and the outputs of the stages 3 are also not seen as connected together. Clarification is requested.

As per claim 13, the same problem exists as discussed in claim 4 above.

As per claims 14-17, these claims are rejected because of the indefiniteness of claim 13.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1-10 and 12-19 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,097,161, issued to Takano et al.

As per claim 1, Takano discloses a semiconductor device (Fig. 3) comprising:

a charge pump circuit (Fig. 3) comprising a plurality of charge pump cascades (23-1 and 23-2), each (for example, 23-1) of the charge pump cascades comprising a plurality of pump stages (T1, …, Tn); and

wherein the plurality of charge pump cascades are driven to pump charge to a common output HVOUT in response to alternate edges of a system clock signal (the input terminals of capacitors C1, ..., Cn in each of the charge pump cascade receive the alternate edges of the system clock signal).

As per claim 2, the semiconductor device of claim 1, further comprising a non overlapping clock signal generator (the circuits 3, 22-1, 22-2 and transistors I1, ..., I4), the non-overlapping clock signal generator generating non-overlapping clock signals in response to alternate rising and falling edges of the system clock signal (Fig. 4, the signals a, b, A and B are non overlapping).

As per claim 3, since the circuit in Fig. 3 is a charge pump circuit, the common output provides an output supply voltage (HVOUT) that is greater than a power supply voltage GND provided to the charge pump circuit.

As per claim 4, Takano discloses a memory device (column 1, line 11) including a charge pump circuit (Fig. 3) comprising:

a first (23-1) and second charge pump cascade (23-2), the first and second charge pump cascade comprising a plurality of charge pump stages (T1, ..., Tn);

each (for example, stage T1) of the plurality of charge pump stages comprising a transistor N1 and a capacitor C1; and

wherein the plurality of charge pump stages pump charge to an output node HVOUT on both a rising edge and a falling edge of a system clock signal (the input terminals of capacitors C1, ..., Cn in each of the charge pump cascade receive the alternate edges of the system clock signal).

As per claim 5, wherein the transistor N1 comprises a PFET configured as a diode (as shown).

As per claim 6, wherein the capacitor C1 comprises a PFET configured as a capacitor (as shown).

As per claim 7, wherein the first and second charge pump cascades receive a power supply voltage GND and are in communication with the output node HVOUT and wherein the output node provides an output supply voltage that is greater than the power supply voltage (because the reference circuit is a charge pump circuit).

As per claim 8, Takano further discloses the circuit comprising a non overlapping clock signal generator (the circuits 3, 22-1, 22-2 and transistors I1, ..., I4) for generating a first and a second phase signal (a and b) in response to opposite phases of the system clock signal wherein the first phase signal drives (2n)th charge pump stage of the first charge pump cascade and (2n +1)th charge pump stage of the second charge pump cascade and wherein the second phase signal drives (2n + 1)th charge pump stage of the first charge pump cascade and (2n)th charge pump stage of the second charge pump cascade, n being an integer greater than or equal to zero (the connections of the two input lines to the capacitors C1, ..., Cn in each of the first and second charge pump cascaded met the recited limitations).

As per claim 9, Takano discloses a charge pump (Fig. 3) comprising:

a first (23-1) and a second pump cascade (23-2) coupled in parallel (as shown) to an output node HVOUT;

the first and the second pump cascades comprising a plurality of pump stages (T1, ..., Tn) coupled in series (as shown);

wherein (2n)th pump stage of the first pump cascade (23-1) is coupled to receive a first clock signal and (2n+l)th pump stage of the first pump cascade is coupled to receive a second clock signal, n being an integer greater than or equal to zero (capacitors C2, ..., C2n receive the first clock signal a and capacitors C1, ..., C(2n+1) receive the second clock signal b);

wherein (2n)th pump stage of the second pump cascade (23-2) is coupled to receive the second clock signal and (2n +1)th pump stage of the second pump cascade is coupled to receive the first clock signal, n being an integer greater than or equal to zero (capacitors C2, ..., C2n receive the second clock signal a and capacitors C1, ..., C(2n+1) receive the first clock signal b); and

wherein the output node HVOUT receives charge pumped by the first and the second pump cascades and provides an output supply voltage HVOUT that is greater in magnitude than the power supply voltage GND.

As per claim 10, wherein each pump stage comprises a PFET configured as a diode N1 and a PFET configured as a capacitor C1.

As per claim 12, Takano discloses a charge pump (Fig. 3) for generating a high voltage supply HVOUT comprising:

a first pump cascade (23-1) comprising multiple charge pump stages (T1, ..., Tn), each charge pump stage in the first pump cascade being driven by a first plurality of clock signals (applied to the capacitors C1, ..., Cn of the first charge pump cascade);

a second pump cascade (23-2) comprising multiple charge pumps stages (T1, ..., Tn), each charge pump stage in the second pump cascade being driving by a second plurality of clock signals (applied to the capacitors C1, ..., Cn of the second charge pump cascade);

a non-overlapping clock signal generator (the circuits 3, 22-1, 22-2 and transistors I1, ..., I4) for generating the first and second plurality of clock signals in response to transitions in a system clock signal, each of the clock signals of the second plurality of clock signals having opposite phases to each of the clock signals of the first plurality of clock signals (see Fig. 4); and

wherein final charge pump stages of the first and second pump cascades are coupled in parallel (as shown, Tn stages of the first and second are connected in parallel) to provide the high voltage supply HVOUT.

As per claims 13-17, these claims are rejected for the same reasons noted in claims 1 and 5-8, respectively.

As per claims 18-19, these claims are merely method to operate a charge pump circuit having elements and connected as discussed in claim 1 above, since Takano teaches the circuit, he inherently teaches the recited methods to operate the circuit.

Allowable Subject Matter

9. Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 11 is allowable because the prior art of record fails to disclose or suggest a charge pump circuit which includes first and second pump cascades wherein each includes a plurality of pump stages and the first pump stage includes a thin oxide PFET configured as a diode and a thin oxide PFET configured as a capacitor.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent Nos. 6,373,328, 4,839,787, 6,037,622 and 5,625,544 disclose charge pump circuits which include a plurality of charge pump cascades and many of the recited claims read on the charge pump circuits disclosed in these patents .

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 703-306-9179. The examiner can normally be reached on Monday - Thursday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Minh Nguyen
Examiner
Art Unit 2816

MN
February 4, 2003